What is claimed is:

1. A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) preparing a semiconductor wafer which has been divided into a plurality chip regions each having a semiconductor integrated circuit formed thereover, and has, formed over the main surface of the wafer, a plurality of first electrodes to be electrically connected with the semiconductor integrated circuit;

(b) preparing a first card for retaining a first sheet, which has a plurality of contact terminals to be brought into contact with the first electrodes and interconnects to be electrically connected with the contact terminals, so as to cause the tip portions of the contact terminals to protrude toward the main surface of the semiconductor wafer; and

(c) bringing the contact terminals into contact with the first electrodes to perform an electrical test of the semiconductor integrated circuit device,

wherein the tip portions of the contact terminals are disposed over a first surface of the first sheet, and a plurality of second electrodes to be electrically connected with the interconnects are disposed over a second surface which is opposite to the first surface of the first sheet,

wherein the first card has a plurality of connection mechanisms to be electrically connected to the second electrodes and pushing mechanisms for pushing the contact

terminals toward the first electrodes,

wherein the connection mechanisms each comprises: an elastic contact needle for pushing the second electrodes by a load generated upon contact of the contact terminals with the first electrodes; and a retainer member for retaining the contact needle and is disposed to get in touch with the second electrodes over the second surface of the first sheet,

wherein each of the pushing mechanisms is formed by successively stacking a first elastic material, a pushing member and a second elastic material one after another from the side of the first sheet and is disposed above the contact terminals over the second surface of the first sheet, and

wherein any one of the pushing mechanisms pushes at least one of the contact terminals.

2. A fabrication method of a semiconductor integrated circuit device according to Claim 1, wherein the pushing mechanism is disposed over each of the contact terminals over the second surface of the first sheet, and any one of the pushing mechanisms pushes one of the contact terminals.

3. A fabrication method of a semiconductor integrated circuit device according to Claim 1, wherein a first reinforcing member is formed in a region of the second surface of the first sheet in which at least the second electrodes are not disposed, and the semiconductor wafer and the first reinforcing member each has a first linear expansion coefficient.

4. A fabrication method of a semiconductor integrated circuit device according to Claim 3, wherein the semiconductor wafer has silicon as a main component and the first reinforcing member has, as a main component, 42 alloy, silicon or a material having a linear expansion coefficient almost equal to that of silicon.

5. A fabrication method of a semiconductor integrated circuit device according to Claim 1, wherein the first elastic material and the second elastic material change their shapes when a pressure is applied by pushing of the contact terminals against the first electrodes so as to absorb the gaps between the tip portions of the contact terminals and the first electrodes.

6. A fabrication method of a semiconductor integrated circuit device according to Claim 1, wherein the elastic modulus of the first elastic material is smaller than that of the second elastic material.

7. A fabrication method of a semiconductor integrated circuit device according to Claim 1, wherein over the second surface of the first sheet, any two adjacent second electrodes are separated with a first space wider than a space between any two adjacent tip portions of the contact terminals, and the first space between any two adjacent second electrodes is set uniform.

8. A fabrication method of a semiconductor integrated circuit device according to Claim 1, wherein the main surface

of the semiconductor wafer is divided into a plurality of first regions, each of the chip regions is disposed in any one of the first regions and the step (c) is performed for each of the first regions.

9. A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) preparing a semiconductor wafer which has been divided into a plurality chip regions each having a semiconductor integrated circuit formed thereover, and has, formed over the main surface, a plurality of first electrodes to be electrically connected with the semiconductor integrated circuit;

(b) preparing a first card for retaining a first sheet, which has a plurality of contact terminals to be brought into contact with the first electrodes and interconnects to be electrically connected with the contact terminals, so as to cause the tip portions of the contact terminals to protrude toward the main surface of the semiconductor wafer; and

(c) bringing the contact terminals into contact with the first electrodes to perform an electrical test of the semiconductor integrated circuit device,

wherein the tip portions of the contact terminals are disposed over a first surface of the first sheet, and a plurality of second electrodes to be electrically connected with the interconnects are disposed over a second surface which is opposite to the first surface of the first sheet,

wherein the first card has a plurality of connection mechanisms to be electrically connected to the second electrodes,

wherein the connection mechanisms each comprises: an elastic contact needle for pushing the second electrodes by a load generated upon contact of the contact terminals with the first electrodes; and a retainer member for retaining the contact needle and is disposed to get in touch with the second electrodes over the second surface of the first sheet, and

wherein the probe needle pushes the second electrodes before the contact terminals are brought into contact with the first electrodes.

10. A fabrication method of a semiconductor integrated circuit device according to Claim 9, wherein a first reinforcing member is formed in a region of the second surface of the first sheet in which at least the second electrodes are not disposed, and the semiconductor wafer and the first reinforcing member each has a first linear expansion coefficient.

11. A fabrication method of a semiconductor integrated circuit device according to Claim 10, wherein the semiconductor wafer has silicon as a main component and the first reinforcing member has, as a main component, 42 alloy, silicon or a material having a linear expansion coefficient almost equal to that of silicon.

12. A fabrication method of a semiconductor integrated

circuit device according to Claim 9, wherein over the second surface of the first sheet, any two adjacent second electrodes are separated with a first space wider than a space between any adjacent two tip portions of the contact terminals, and the first space between any two adjacent second electrodes is set uniform.

13. A fabrication method of a semiconductor integrated circuit device according to Claim 9, wherein the main surface of the semiconductor wafer is divided into a plurality of first regions, each of the chip regions is disposed in any one of the first regions and the step (c) is performed for each of the first regions.

14. A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) preparing a semiconductor wafer which has been divided into a plurality chip regions each having a semiconductor integrated circuit formed thereover, and has, formed over the main surface, a plurality of first electrodes to be electrically connected with the semiconductor integrated circuit;

(b) preparing a first card for retaining a first sheet, which has a plurality of contact terminals to be brought into contact with the first electrodes and interconnects to be electrically connected with the contact terminals, so as to cause the tip portions of the contact terminals to protrude toward the main surface of the semiconductor wafer; and

(c) bringing the contact terminals into contact with the first electrodes to perform an electrical test of the semiconductor integrated circuit device,

wherein the tip portions of the contact terminals are disposed over a first surface of the first sheet, and a plurality of second electrodes to be electrically connected with the interconnects are disposed over a second surface which is opposite to the first surface of the first sheet,

wherein the first card has a plurality of connection mechanisms to be electrically connected to the second electrodes,

wherein the connection mechanisms each comprises: an elastic contact needle for pushing the surface of the second electrodes by a load generated upon contact of the contact terminals with the first electrodes; and a retainer member for retaining the contact needle, and is disposed to get in touch with the second electrodes over the second surface of the first sheet, and

wherein the surface of each of the second electrodes to be brought into contact with the contact needle has been planarized.

15. A fabrication method of a semiconductor integrated circuit device according to Claim 14, wherein a first reinforcing member is formed in a region of the second surface of the first sheet in which at least the second electrodes are not disposed, and the semiconductor wafer and the first

reinforcing member each has a first linear expansion coefficient.

16. A fabrication method of a semiconductor integrated circuit device according to Claim 15, wherein the semiconductor wafer has silicon as a main component and the first reinforcing member has, as a main component, 42 alloy, silicon or a material having a linear expansion coefficient almost equal to that of silicon.

17. A fabrication method of a semiconductor integrated circuit device according to Claim 14, wherein over the second surface of the first sheet, any two adjacent second electrodes are separated with a first space wider than a space between any adjacent two tip portions of the contact terminals, and the first space between any two adjacent second electrodes is set uniform.

18. A fabrication method of a semiconductor integrated circuit device according to Claim 14, wherein the main surface of the semiconductor wafer is divided into a plurality of first regions, each of the chip regions is disposed in any one of the first regions, and the step (c) is performed for each of the first regions.